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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(in as many sheets as necessary)</i>				Application Number	10/606,031
				Filing Date	June 25, 2003
				First Named Inventor	Paul Master
				Art Unit	2622
				Examiner Name	Nelson D. Hernandez
Sheet	1	of	4	Attorney Docket Number	046301/101000

U.S. PATENT DOCUMENTS

Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)				
/NDHH/ <						

Examiner Signature	/Nelson D. Hernandez/	Date Considered	07/29/2009
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U.S. PUBLISHED PATENT DOCUMENTS

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(see as many sheets as necessary)

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	75.	US 2002/0184275	A1	12-05-2002	Dutta et al.	
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	78.	US 2003/0229864	A1	12-11-2003	Watkins	
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	80.	US 2004/0133745	A1	07-08-2004	Ramchandran	
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NDHH/	84.	WO	00/69073	A1	Wasson		

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NDHH/	85.	Altera Apex 20K 1999				
	86.	Andraka Consulting Group, "Distributed Arithmetic," Obtained from: http://www.fpga-guru.com/distrib.htm (1998-2000)				
	87.	Computer Organization and Design 2 nd Edition, Hennessy, Morgan Kaufmann Publishers, pp. 569–70 (1998)				
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	89.	Hanna et al., "A Normalized Backpropagation Learning Algorithm for Multilayer Feed-Forward Neural Adaptive Filters," <i>Neural Networks for Signal Processing XI</i> , Proceedings of the 2001 IEEE Signal Processing Society Workshop pp. 63–72 (Sept 2001)				
	90.	Janweijer et al., "A Compact Robin Using the SHarc (CRUSH)," Obtained from: http://www.nikhef.nl/~peterj/CRUSH/CRUSH-hw.pdf (Sept 1998)				
	91.	Rajagopalan et al., "A Flexible Multiplication Unit for an FPGA Logic Block," <i>Circuits and Systems</i> 4:546–9 (2001)				
	92.	Xilinx Data Book 1998				
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/NDHH/	94.	Xilinx Virtex 2.2 2000	

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